## Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1 and 20 have been amended. No claims have been cancelled. Therefore, claims 1-24 are presented for examination.

Claims 1-4, 6-8, 1-12, 14-16 and 20-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wilde (U.S. Patent No. 5,828,382) in view of Cosman (U.S. Patent No. 5,651,104). Applicants submit that the present claims are patentable over Wilde and Cosman.

Wilde discloses a graphics system coupled to a system bus of a computer system. The computer system includes a central processing system 150, system cache memory, main memory, and a graphics processor. A central processor (CPU) is coupled to the bus to process data and information which may include graphics data and information utilized by the graphics processor of the present invention. The graphics processor includes the capabilities to rasterize graphics data or information from the CPU to either a display memory or a main memory depending on the address offset in the display information. The display memory may include a frame buffer for storing the XY information for graphics primitives rendered to display unit, and a Z-buffer for storing depth information representing depth values of such graphics primitives. See Wilde at col. 4, ll. 3-53. Nevertheless, Wilde does not disclose or suggest a unified graphics cache coupled to a graphics core and a CPU to store a supersampled image.

Cosman discloses a computer graphics system that is defined using supersampling of multi-level pixel characteristic data. The system provides a detailed anti-aliased display of the texture on surfaces defined at oblique angles within the model space while providing simple real time controls to control the amount of extra processing required for the supersampling. A sampling path is defined within a projected pixel footprint on a textured surface defined in model space. These sample points are mapped to levels of detail and

locations within a texture MIP map. The level of detail and supersampling locations are calculated for each pixel that the polygon influences. The sampled texture data is blended forming a single texture value for that pixel. This texture value is blended with other characteristics of the pixel to form the pixel data that is displayed on a display unit. See Cosman at Abstract. However, Cosman does not disclose or suggest a unified graphics cache coupled to a graphics core and a CPU to store a supersampled image.

Claim 1 recites a unified graphics cache coupled to a graphics core and a CPU, to store a supersampled image. As discussed above, nowhere in Wilde or Cosman is there disclosed a unified graphics cache. Wilde discloses as system cache coupled to the CPU. However, the system cache is not a graphics cache since it is not used to store image data. Moreover, there is no disclose of a unified graphics cache to store a supersampled image. Since neither Wilde nor Cosman disclose or suggest a unified graphics cache coupled to a graphics core and a CPU to store a supersampled image, any combination of Wilde and Cosman would also not disclose such a limitation. Therefore, claim 1 is patentable over Wilde in view of Cosman.

Claims 2-10 depend from claim 1 and include additional limitations. Accordingly, claims 2-10 are also patentable over Wilde in view of Cosman.

Claim 11 recites rendering polygons of a first tile into a unified graphics cache. Thus, for the reasons described above with respect to claim 1, claim 11 is also patentable over Wilde in view of Cosman. Because claims 12-19 depend from claim 11 and include additional limitations, claims 12-19 are also patentable over Wilde in view of Cosman.

Claim 20 recites a unified graphics cache coupled to a graphics core and a CPU, to store a supersampled image. Therefore, for the reasons described above with respect to claim 1, claim 11 is also patentable over Wilde in view of Cosman. Since claims 21-24 depend from claim 11 and include additional limitations, claims 21-24 are also patentable over Wilde in view of Cosman.

Claims 9, 13 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wilde in view of Cosman as applied to claims 1, 11 and 20 above and further in view of Pfister et al. (U.S. Patent No. 6,448,968). Applicants submit that the present claims are patentable over Wilde and Cosman even in view of Pfister.

Pfister discloses a method for modeling a representation of a graphic object. A surface of the object is partitioned into a plurality of cells having a grid resolution related to an image plane resolution. A single zero-dimensional surface element is stored in the memory for each cell located on the surface of the object. The surface elements in adjacent cells are connected by links, and attributes of the portion of the object contained in the cell are assigned to each surface element and each link. The location of the attributed surface elements can be moved according to forces acting on the object. See Pfister at Abstract.

However, Pfister does not disclose or suggest a unified graphics cache coupled to a graphics core and a CPU to store a supersampled image. As described above, Wilde and Cosman also do not disclose or suggest such a limitation. Accordingly, any combination of Wilde and Cosman and Pfister would also not disclose or suggest a unified graphics cache coupled to a graphics core and a CPU to store a supersampled image. Thus, the present claims are patentable over Wilde, Cosman and Pfister.

Claims 10 and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wilde in view of Cosman and further of Pfister et al. as applied to claims 1-9 and 11-17 above, further in view of Li et al. (U.S. Patent No. 5,860,060). Applicants submit that the present claims are patentable over Wilde, Cosman and Pfister even in view of Li.

Li discloses a data processing device that uses a portion of random access memory as an output buffer for holding a portion of a stream of PCM data which is to be output to a digital to analog converter. D/A forms a left analog channel and a right analog channel for speaker subsystems and. The PCM data stream is stored in the output buffer so that PCM data samples which pertain to the left channel are stored at even address and PCM data samples which pertain to the right channel are stored at odd address. Control circuitry

monitors direct memory access (DMA) transfers which transfer PCM data samples to PCM serializer. By comparing the address of each DMA transfer to a left/right channel signal from the D/A, the control circuitry can verify that channel synchronization is correct. If a synchronization error is detected, an channel synchronization error correction procedure is invoked. See Li at Abstract.

Nonetheless, Li does not disclose or suggest a unified graphics cache coupled to a graphics core and a CPU to store a supersampled image. As discussed above, neither Wilde, Cosman, nor Pfister disclose or suggest a unified graphics cache coupled to a graphics core and a CPU to store a supersampled image. Therefore, any combination of Wilde, Cosman, Pfister and Li would also not disclose such limitations. Thus, the present claims are patentable over Wilde, Cosman in view of Pfister and Li.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: December 12, 2003

Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980